AMENDMENTS TO THE CLAIMS

Claims 1-30 (Cancelled)

31. (Previously Presented) A method of planarizing a layer of semiconductor material formed on a wafer, the wafer having a top surface, the top surface having a first region and a second region that lies above the first region, the first region being equal to a lowest part of the top surface, the second region being equal to a highest part of the top surface, the method comprising:

forming a layer of first material to contact the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first region and a second region that lies above the first region of the layer of first material, the first region of the layer of first material being equal to a lowest part of the top surface of the layer of first material, the second region of the layer of first material being equal to a highest part of the top surface of the layer of first material;

forming a layer of second material to contact the top surface of the layer of first material, the layer of second material having a top surface, the top surface of the layer of second material having a first region and a second region that lies above the first region of the layer of second material, the first region of the layer of second material being equal to a lowest part of the top surface of the layer of second material, the second region of the layer of second material being equal to a highest part of the top surface of the layer of second material, the first region of the top surface of the layer of second material lying above the second region of the top surface of the layer of first material; and

performing a chemical-mechanical polish of the layer of second material and the layer of first material, the chemical-mechanical polish continuing until the layer of second material has been substantially all removed from the layer of first material, thereby forming the layer of first material to have a substantially planar top surface, the substantially planar top surface of the layer of first material lying over the first region and the second region of the top surface of the wafer.

32. (Previously Presented) The method of claim 31 wherein:

the substantially planar top surface of the layer of first material has a first thickness over the second region of the top surface of the wafer, and

the layer of first material is formed such that the first region of the top surface of the layer of first material lies above the second region of the top surface of the wafer by a second thickness that is equal to or greater than the first thickness.

33. (Previously Presented) The method of claim 31 wherein the layer of first material is conductive and electrically connected to a device on the wafer.

34. (Previously Presented) The method of claim 33 wherein the layer of first material is polysilicon.

35. (Previously Presented) The method of claim 34 and further comprising doping the layer of polysilicon prior to forming the layer of second material.

36. (Previously Presented) The method of claim 33 wherein the layer of second material is non-conductive.

37. (Previously Presented) The method of claim 31 wherein the chemical-mechanical polish removes the layer of first material and the layer of second material at approximately a same rate.

38. (Previously Presented) The method of claim 31 and further comprising forming a layer of third material over the substantially planar top surface of the layer of first material, the third layer of material lying above and being vertically spaced apart from the second region of the top surface of the wafer.

39. (Previously Presented) The method of claim 38 wherein the layer of third material is a mask.

40. (Previously Presented) The method of claim 38 wherein:

the substantially planar top surface of the layer of first material includes doped polysilicon; and

the layer of third material lowers a resistance of doped polysilicon.

41. (Previously Presented) The method of claim 40 and further comprising forming a mask on the layer of third material.

42. (Currently Amended) A method of planarizing a layer of semiconductor material formed on a wafer, the wafer having a top surface, the top surface having a first region and a second region that lies above the first region, the first region being equal to a lowest part of the top surface, the second region being equal to a highest part of the top surface, the method comprising:

conformally forming a layer of first material to contact the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first region and a second region that lies above the first region of the layer of first material, the first region of the layer of first material being equal to a lowest part of the top surface of the layer of first material, the second region of the layer of first material being equal to a highest part of the top surface of the layer of first material;

forming a layer of second material to contact and adhere to the top surface of the layer of first material; and

performing a chemical-mechanical polish of the layer of second material and the layer of first material, the chemical-mechanical polish continuing until the layer of second material has been substantially all removed from the layer of first material at which time the layer of first material has a substantially planar top surface, the substantially planar top surface of the layer of first material lying over the second region of the top surface of the wafer.

43. (Previously Presented) The method of claim 42 wherein:

the substantially planar top surface of the layer of first material has a first thickness over the second region of the top surface of the wafer, and

the layer of first material is formed such that the first region of the top surface of the layer of first material lies above the second region of the top surface of the wafer by a second thickness that is equal to or greater than the first thickness.

44. (Previously Presented) The method of claim 42 wherein the layer of first material is conductive and electrically connected to a device on the wafer.

45. (Previously Presented) The method of claim 44 wherein the layer of first material is polysilicon.

46. (Previously Presented) The method of claim 45 and further comprising doping the layer of polysilicon prior to forming the layer of second material.

47. (Previously Presented) The method of claim 44 wherein the layer of second material is non-conductive.

48. (Previously Presented) The method of claim 42 wherein the chemical-mechanical polish removes the layer of first material and the layer of second material at approximately a same rate.

49. (Previously Presented) The method of claim 42 and further comprising forming a layer of third material over the substantially planar top surface of the layer of first material, the third layer of material lying above and being vertically spaced apart from the second region of the top surface of the wafer.

50. (Previously Presented) The method of claim 49 wherein the layer of third material is a mask.

51. (Previously Presented) The method of claim 49 wherein:

the substantially planar top surface of the layer of first material includes doped polysilicon; and

the layer of third material lowers a resistance of doped polysilicon.

52. (Previously Presented) The method of claim 51 and further comprising forming a mask on the layer of third material.